VASA: Vector AES Instructions for Security Applications

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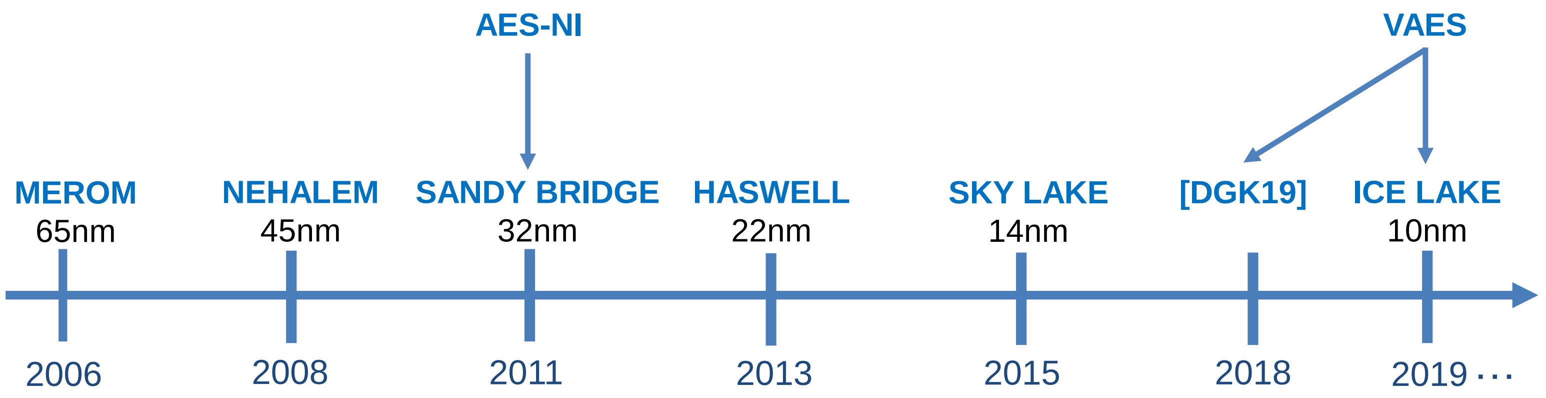
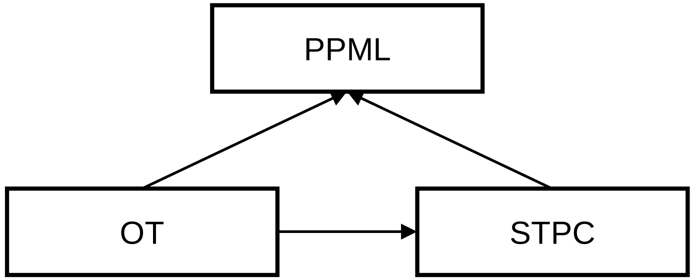
ENCRYPTO CRYPTOGRAPHY AND PRIVACY ENGINEERING

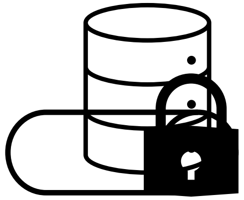


Motivation – Security Applications

- AES is the most ubiquitous symmetric cipher and used in many applications
  - Disk encryption / Transmission encryption
  - Post-quantum signature schemes [DGK21]
  - Secure two-party computation (STPC)
- STPC protocols are implemented with AES



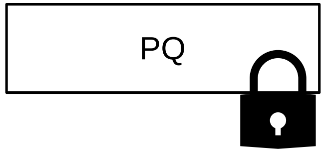
Motivation - Some Use Cases of Parallel AES



Disk Encryption / Transmission Encryption [DGK19]

Trivial parallelism → Solve once

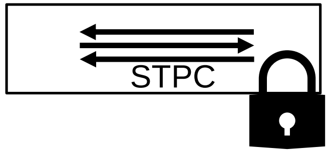
Difficulty?



Post-Quantum Signatures [DG19a, DG19b, DGK21]

Accelerate PRFs → and PRGs

This work:



Secure Two Party Computation

Complex data dependencies from circuits →

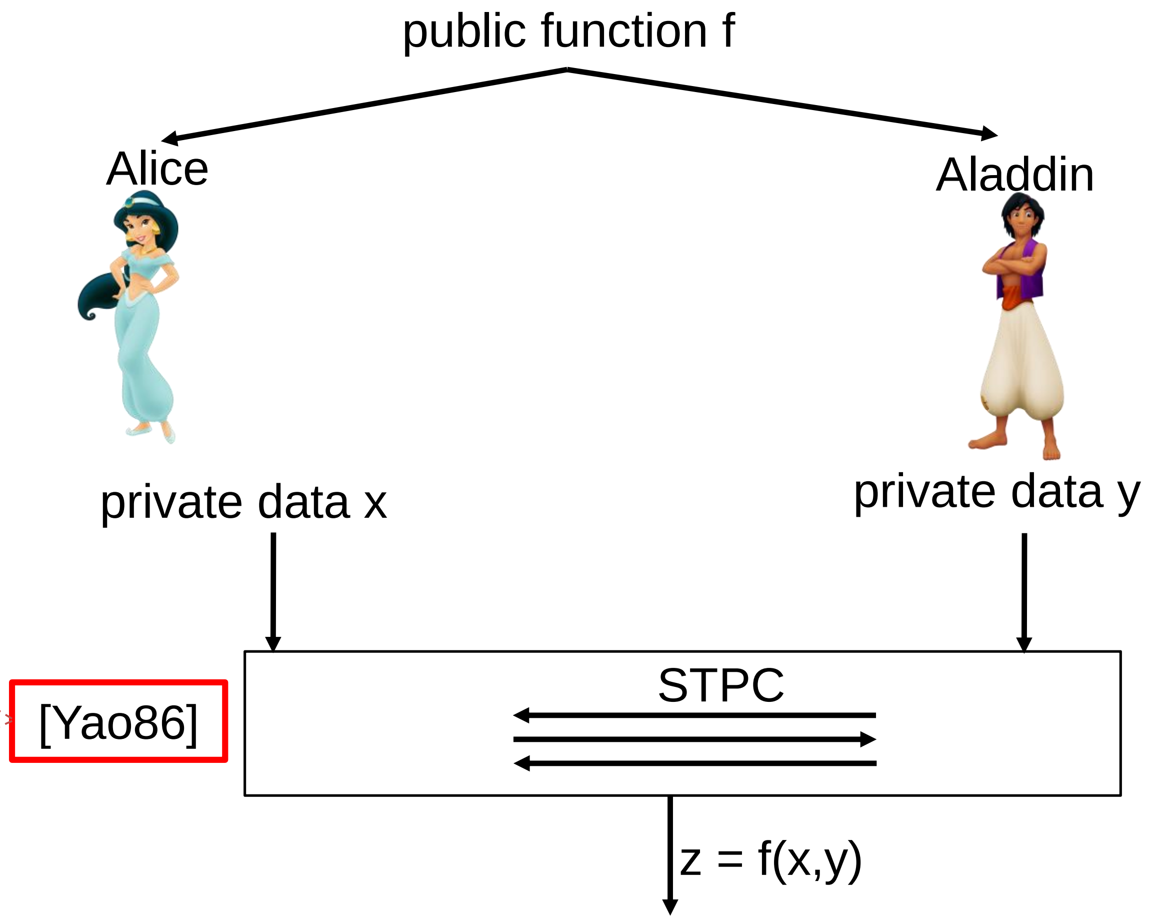
Our challenge: Batch enough independent AES calls together for the AES hardware units
Our goal: Improve efficiency of STPC protocol implementations using VAES

Preliminaries - Secure Two-Party Computation (STPC)

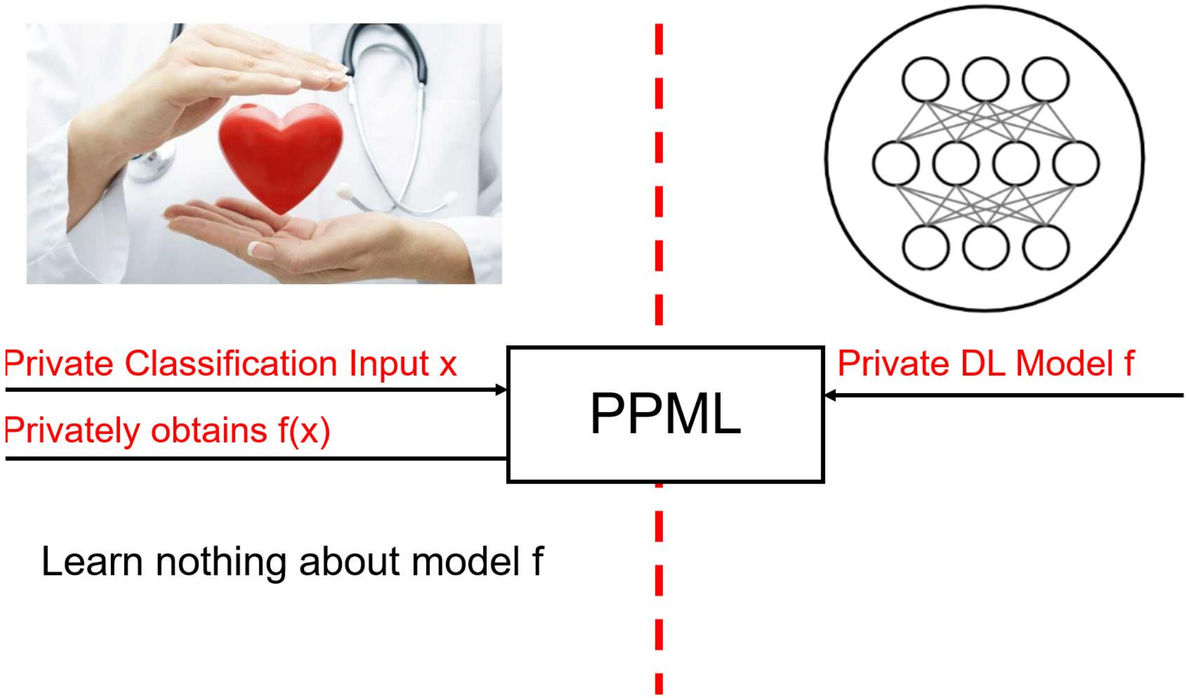
- Compute arbitrary function f
- On private data x, y
- Without trusted third party
- Reveal nothing but the result z = f(x,y)

Free-XOR [KS08]

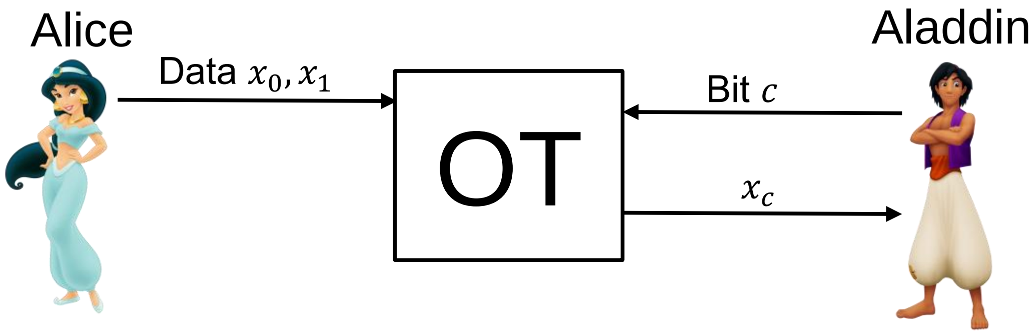
Fixed-key Garbling [BHK13]
Via AES



Privacy-preserving Machine Learning (PPML) and Oblivious Transfer (OT)

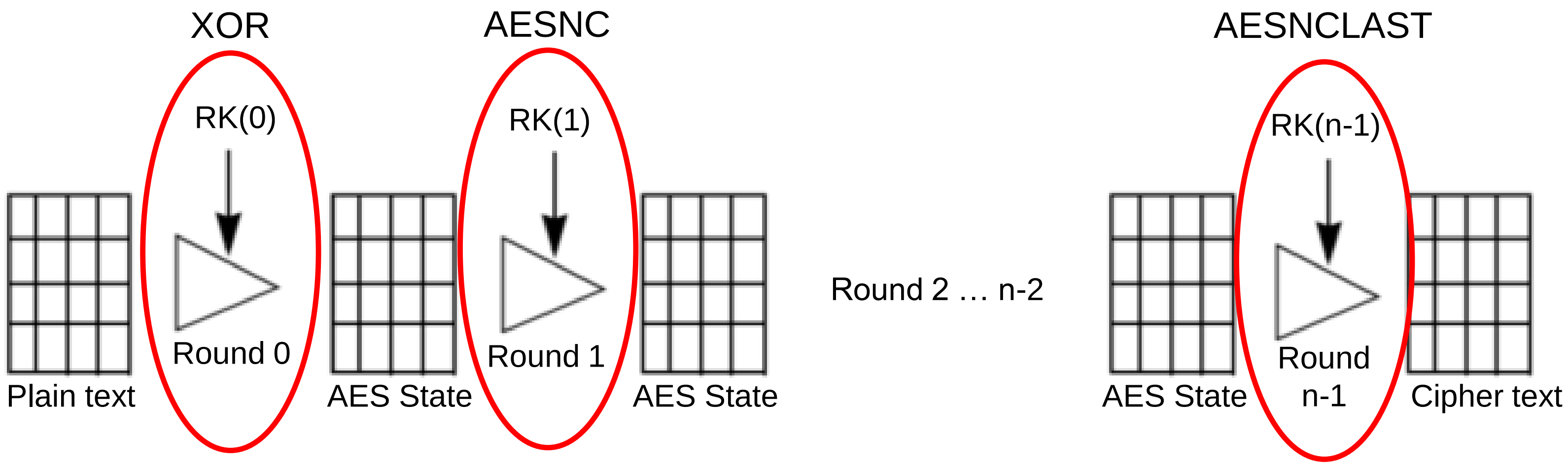


Privacy-preserving Machine Learning (PPML)



Oblivious Transfer (OT) Protocol

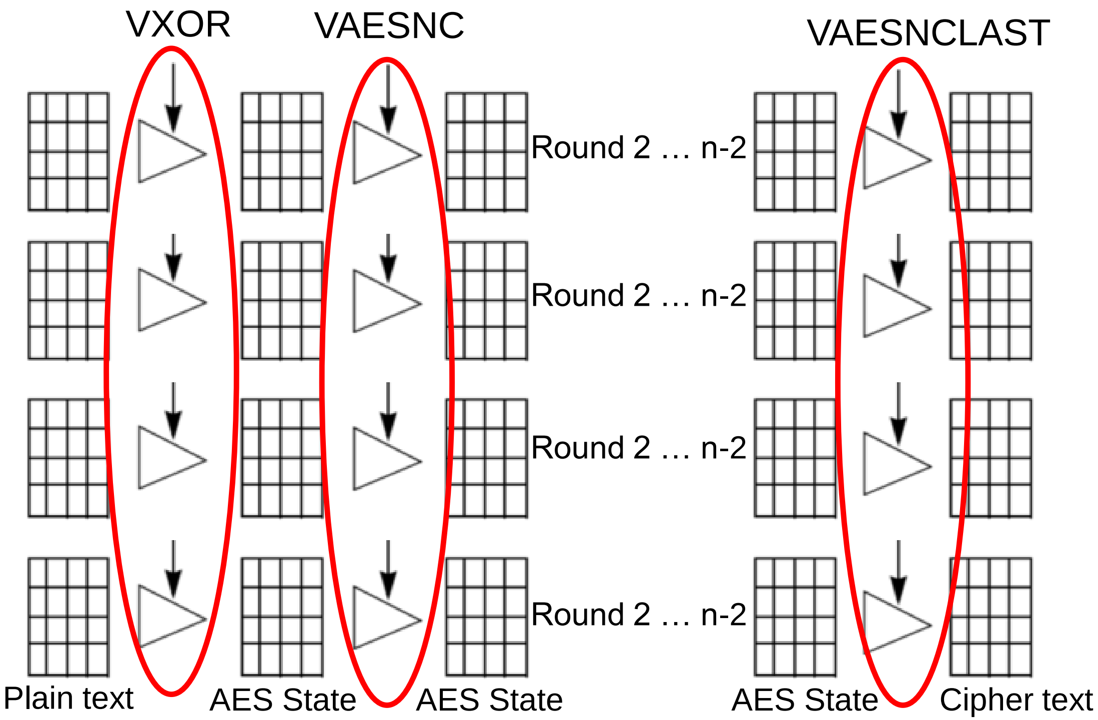
AES



AES-128: n=10
AES-192: n=12
AES-256: n=14

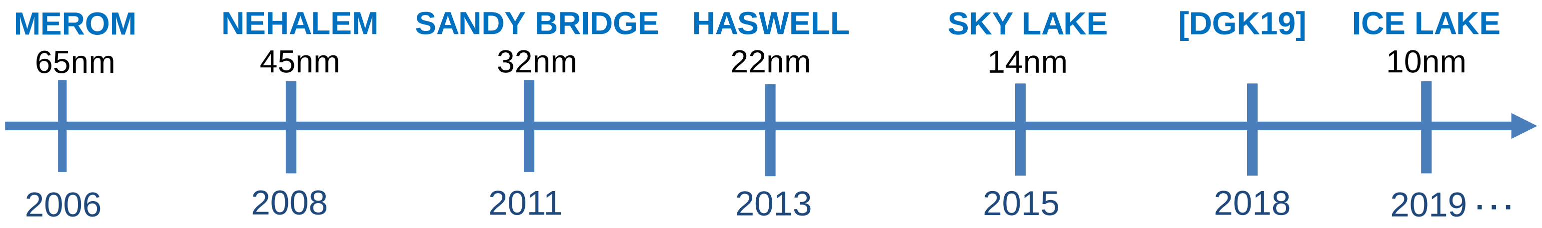
Vectorized AES (VAES) [DGK19]

- Importance of batching data and microarchitectural properties [DGK19]
  - Block ciphers: AES-CTR, AES-CBC, AES-GCM, and AES-GCM-SI.
    - Up to 4×performance improvements



AES-NI vs. VAES [Fog]

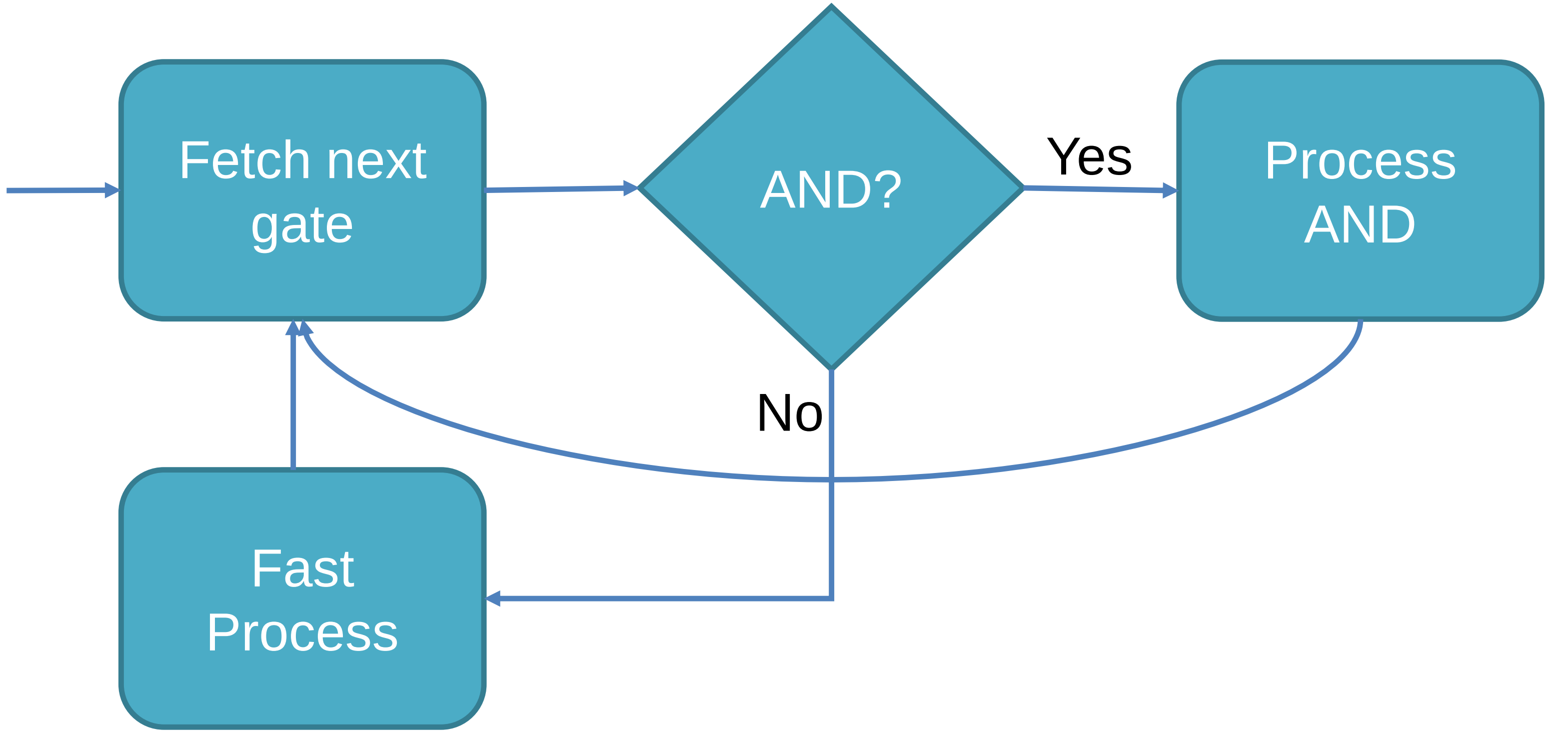
Year	Architecture	Acceleration	Width [op]	Latency [cycles]	Throughput [CPI]	Minimal Batch Size
2013	Haswell	AES-NI	1	7	1	7
2015	Sky lake	AES-NI	1	4	1	4
2019	Ice lake	VAES	1/2/4	3/3/3	0.5/0.5/1	6/12/12



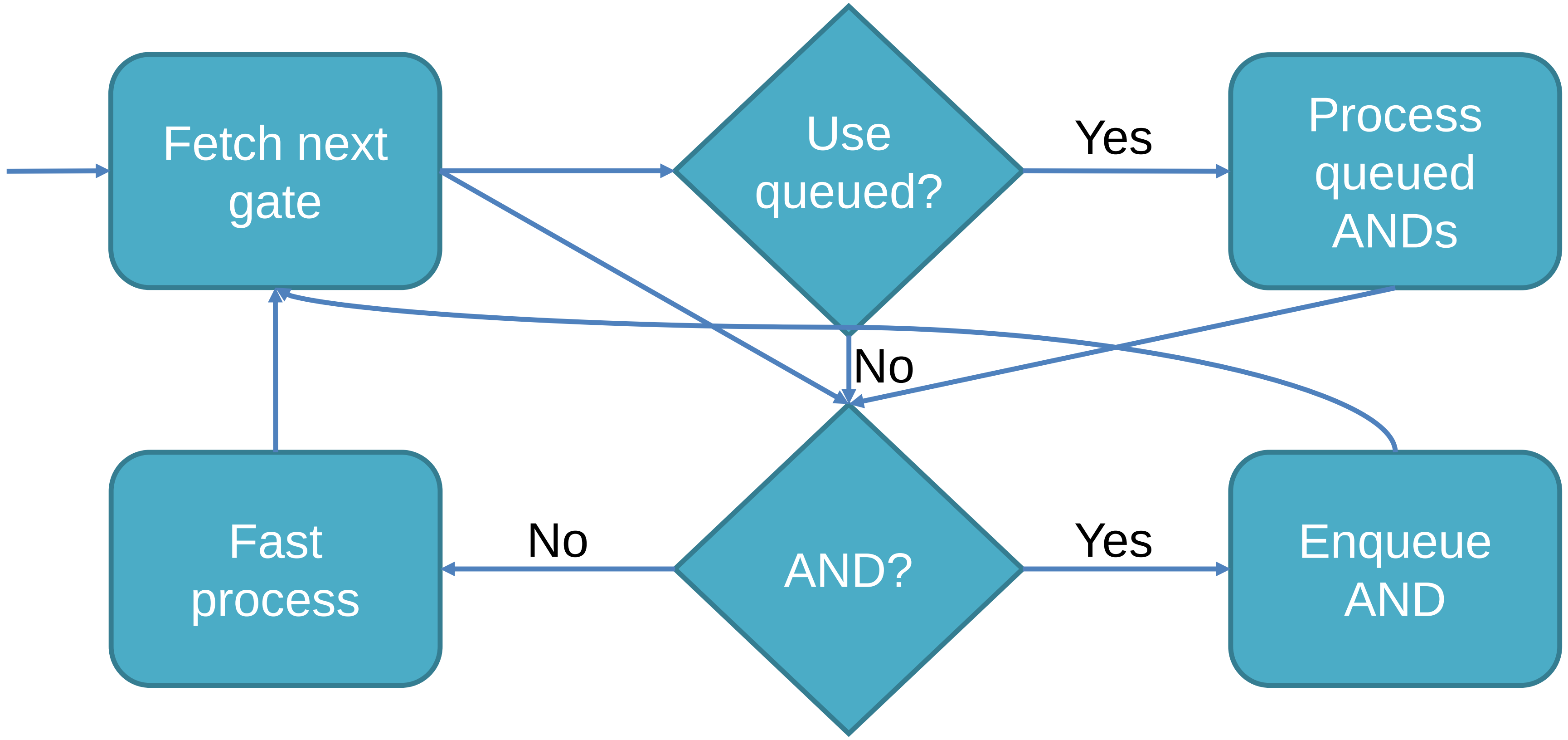
Our Contributions

- Automatic batch identification and computation techniques for efficient use of AES in complex security applications
- First performance measurements for VAES in the area of STPC
  - STPC frameworks: ABY [DSZ15], EMP-OT [Emptool]
  - PPML framework: CrypTFlow2 [RRKC+20]
- Open-source implementation at https://encrypto.de/code/VASA

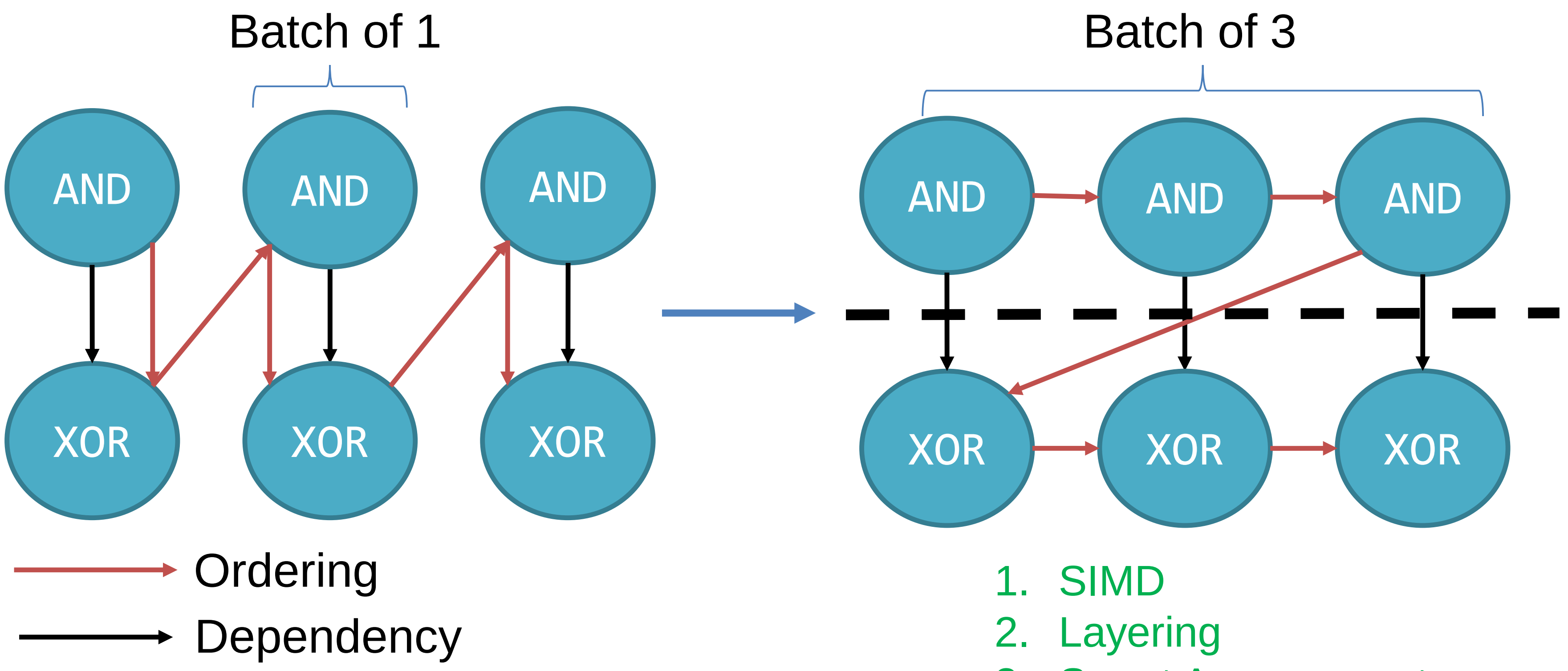
Parallelization - Baseline Scenario



Parallelization - Dynamic Batching



Parallelization - Static Batching



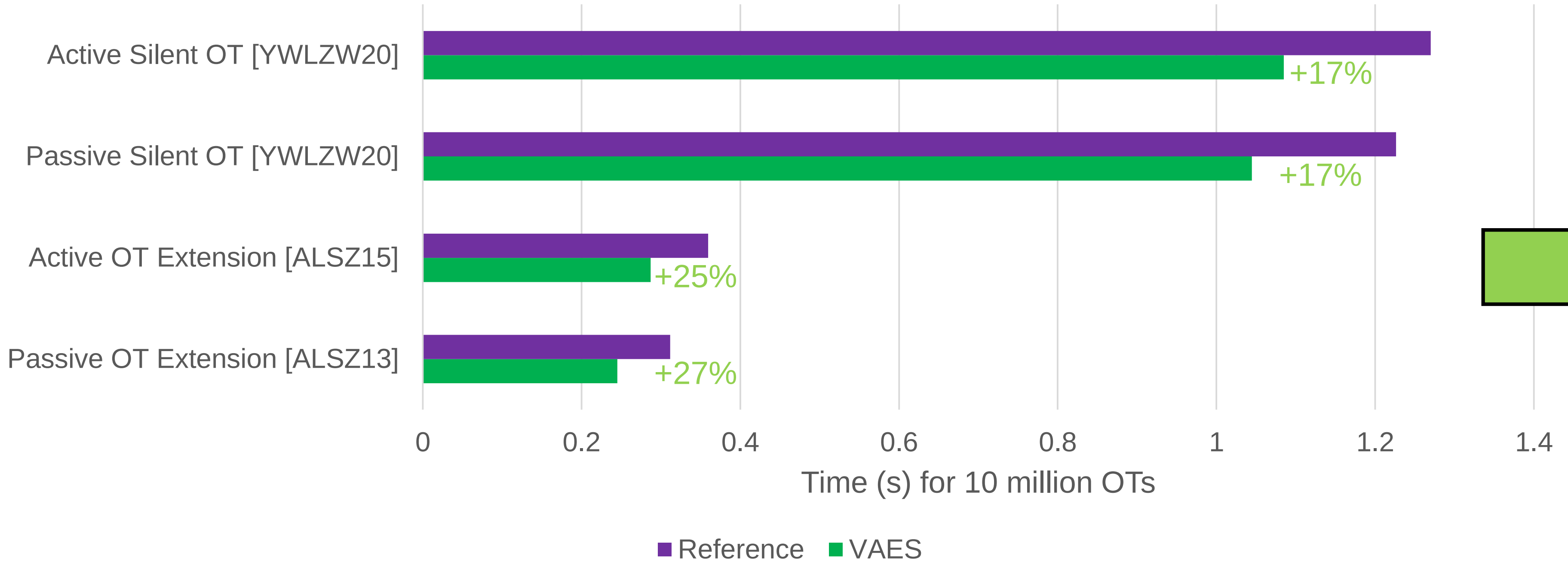
1. SIMD
2. Layering
3. Smart Arrangement

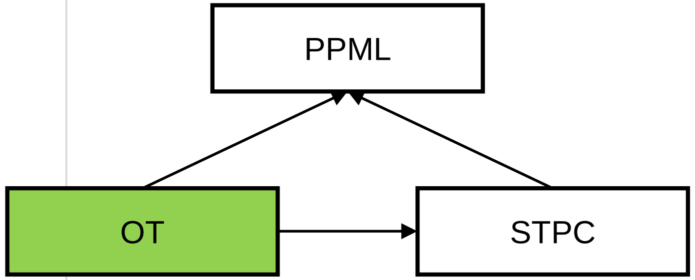
Benchmarking – Evaluation Platform

- Apple Macbook Pro
  - Intel Core i7-1068NG7, 2x16GB dual rank RAM

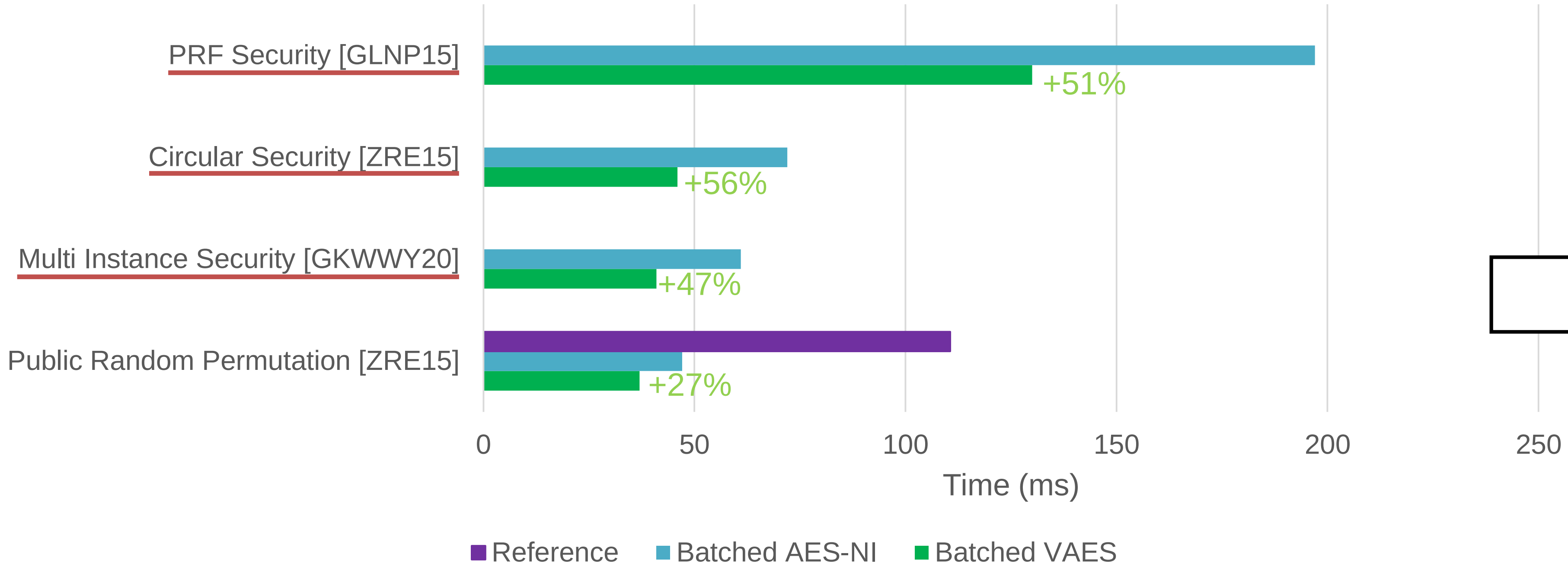
- Oblivious Transfer in EMP [EMPtool]
- Yao's Garbled Circuit in ABY [DSZ15]
- PPML in CrypTFlow2 [RRKC+20]

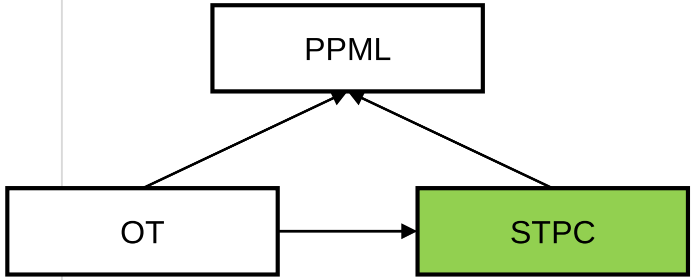
Benchmarking – OT in EMP Framework





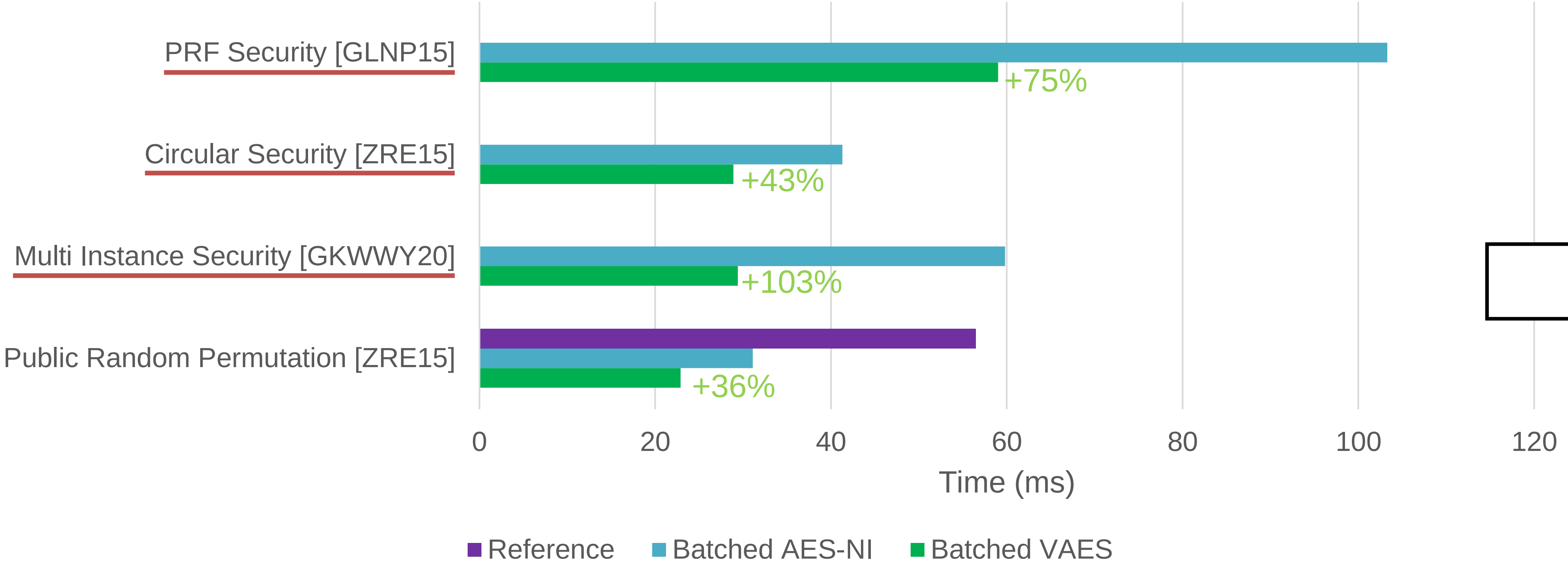
Benchmarking - Yao Garbling in ABY

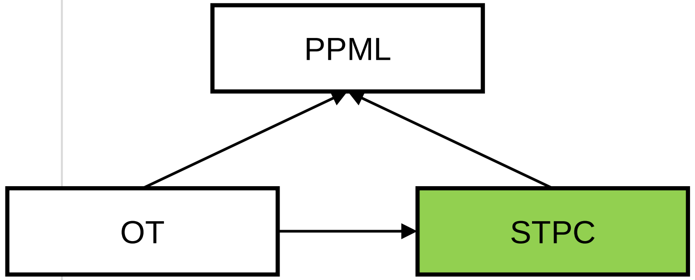




Average runtimes for applications AES, SHA-1, SCS-PSI, and Phasing-PSI.

Benchmarking - Yao Evaluation in ABY





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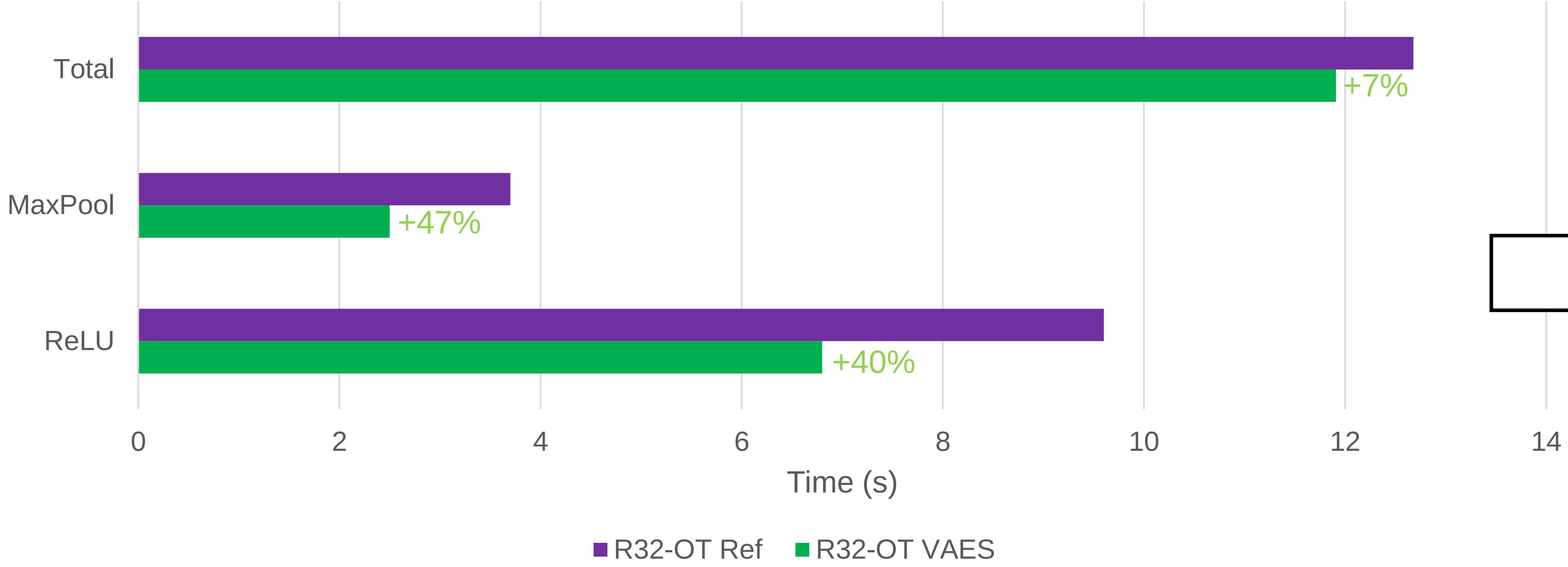
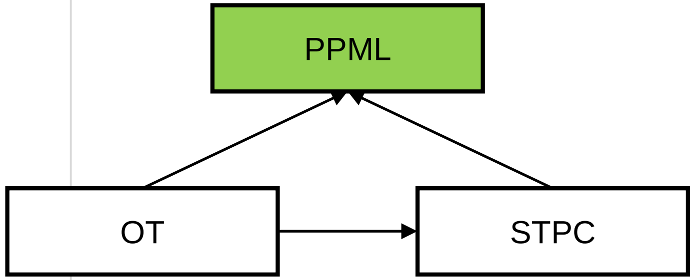
Benchmarking – PPML in CrypTFlow2 Framework





Geometric mean of run-times using the SqueezeNetImgNet, SqueezeNetCIFAR, ResNet50, and DenseNet121 networks.

Conclusion

- ✓ Computation in STPC protocols can be accelerated with VAES
- ✓ Automatic batching of AES calls to the hardware units
- ✓ VAES yields significant performance improvements for parallel circuits

Future Work

- ✓ VAES in further MPC protocols

Thank You!

That was VASA:
Vector AES Instructions for Security Applications

Paper: https://ia.cr/2021/1493

Code: https://encrypto.de/code/VASA

Questions?

https://encrypto.de/yalame

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